Claims

We claim:

1. An integrated photonic-electronic circuit comprising:

an electronic circuit portion comprising at least one group IV semiconductor layer; and

a photonic interface comprising silicon, wherein the photonic interface comprises a coupler for coupling the electronic circuit portion to one or more optical fibers and wherein said photonic interface is at least partially transparent to light with an energy less than the bandgap energy of the group IV semiconductor layer;

wherein said integrated photonic-electronic circuit is integrated on a single chip.

2. The integrated photonic-electronic circuit of claim 1 wherein:

the group IV semiconductor layer comprises silicon.

3. The integrated photonic-electronic circuit of claim 1 wherein:

the group IV semiconductor layer comprises germanium.

4. The integrated photonic-electronic circuit of claim 1 wherein:

the portion of the photonic interface that is at least partially transparent to light with an energy less than the bandgap energy of the group IV semiconductor layer comprises:

elemental silicon.

5. The integrated photonic-electronic circuit of claim 1 wherein:

the single chip is a silicon substrate, silicon on quartz substrate, silicon on sapphire (SOS) substrate or silicon on insulator (SOI) substrate.

6. The integrated photonic-electronic circuit of claim 1 wherein:

the coupler comprises one or more receivers for receiving optical signals from one or more of the optical fibers.

7. The integrated photonic-electronic circuit of claim 6 wherein:

the receiver comprises one or more broad-band couplers.

8. The integrated photonic-electronic circuit of claim 6 wherein:

the receiver comprises one or more detectors.

9. The integrated photonic-electronic circuit of claim 6 wherein:

the receiver further comprises one or more optical filters.

10. The integrated photonic-electronic circuit of claim 9 wherein:

the optical filter is an optical demultiplexer, a waveguide based filter, an Arrayed WaveGuide (AWG) demultiplexer, ring resonator demultiplexer or an add/drop filter.

11. The integrated photonic-electronic circuit of claim 1 wherein the coupler comprises one or more transmitters for transmitting optical signals to one or more of the optical fibers.

12. The integrated photonic-electronic circuit of claim 11 wherein:

the transmitter comprises one or more modulators.

13. The integrated photonic-electronic circuit of claim 11 wherein:

the transmitter comprises one or more broad-band couplers.

14. The integrated photonic-electronic circuit of claim 11 wherein:

the transmitter further comprises one or more optical filters.

15. The integrated photonic-electronic circuit of claim 14 wherein:

the optical filter is an optical demultiplexer, a waveguide based filter, an Arrayed WaveGuide (AWG) demultiplexer, ring resonator demultiplexer, an add/drop filter, an optical multiplexer, an Arrayed WaveGuide multiplexer or an ring resonator multiplexer.

16. The integrated photonic-electronic circuit of claim 11 wherein:

the transmitter further comprises an optical power receiver for receiving optical power from an external optical power source.

17. The integrated photonic-electronic circuit of claim 16 wherein:

the external optical power source may comprise a substantially coherent light source.

18. The integrated photonic-electronic circuit of claim 16 wherein:

the external optical power source may comprise a partially incoherent light source.

19. The integrated photonic-electronic circuit of claim 16 wherein:

the external optical power source may comprise a single wavelength light source.

20. The integrated photonic-electronic circuit of claim 16 wherein:

the external optical power source may comprise a multiple wavelength light source.

21. The integrated photonic-electronic circuit of claim 1 wherein:

light may be transmitted through the integrated photonic-electronic circuit through waveguides comprised of silicon.

22. The integrated photonic-electronic circuit of claim 21 wherein:

the waveguides comprised of silicon are substantially in the plane of the chip.

23. The integrated photonic-electronic circuit of claim 1 wherein:

the electronic circuit portion comprises a processor.

24. The integrated photonic-electronic circuit of claim 1 wherein:

the electronic circuit portion comprises a device selected from the group consisting of: a field programmable gate array (FPGA), a Programmable Logic Devices (PLD), or a Complex Programmable Logic Devices (CPLD).

25. The integrated photonic-electronic circuit of claim 1 wherein:

the electronic circuit portion comprises a memory module.

26. The integrated photonic-electronic circuit of claim 1 wherein:

the electronic circuit portion comprises analog circuits.

27. The integrated photonic-electronic circuit of claim 1 wherein:

the electronic circuit portion comprises radio frequency (RF) circuits.

28. The integrated photonic-electronic circuit of claim 1 wherein:

the electronic circuit portion comprises Complementary Metal Oxide Semiconductor (CMOS) circuits.

29. The integrated photonic-electronic circuit of claim 1 wherein:

the electronic circuit portion comprises Bipolar Complementary Metal Oxide Semiconductor (bi-CMOS) circuits.

30. The integrated photonic-electronic circuit of claim 1 wherein:

the electronic circuit portion comprises Hetero-Junction Biploar Transistor (HBT) circuits.

31. The integrated photonic-electronic circuit of claim 1 wherein:

the electronic circuit portion comprises a memory controller.

32. The integrated photonic-electronic circuit of claim 1 wherein:

the integrated photonic-electronic circuit is reconfigurable.

33. The integrated photonic-electronic circuit of claim 32 wherein:

the photonic interface is reconfigurable.

34. The integrated photonic-electronic circuit of claim 32 wherein:

the integrated photonic-electronic circuit is remotely reconfigurable.

35. The integrated photonic-electronic circuit of claim 32 wherein:

the integrated photonic-electronic circuit is self-reconfiguring.

36. The integrated photonic-electronic circuit of claim 1 wherein:

the integrated photonic-electronic circuit is introspective.

37. The integrated photonic-electronic circuit of claim 1 wherein:

one or more of the optical fibers may be coupled to the top surface of the integrated photonic-electronic circuit.

38. The integrated photonic-electronic circuit of claim 1 wherein:

one or more of the optical fibers may be coupled to the backside surface of the integrated photonic-electronic circuit.

39. The integrated photonic-electronic circuit of claim 1 wherein:

one or more of the optical fibers may be coupled to the edge of the integrated photonic-electronic circuit.

40. The integrated photonic-electronic circuit of claim 1 wherein:

one or more of the optical fibers may be coupled to a surface of the integrated photonic-electronic circuit through a grating coupler.

41. The integrated photonic-electronic circuit of claim 1 further comprising:

one or more electronic interfaces for electronically coupling to one or more electronic interconnects.

42. Integrated photonic-electronic design method comprising the steps of:

generating a design definition comprising an electronic circuit portion and a photonic interface integrated on a single chip, wherein the photonic interface comprises a coupler for coupling the circuit portion to one or more optical fibers and wherein one function of the photonic interface is to optically process light substantially in the plane of the chip; and

verifying the design definition by simulating one or more photonic-electronic models representing the design definition.

43. The integrated photonic-electronic design method of claim 42 wherein:

the electronic circuit portion comprises at least one group IV semiconductor layer.

44. The integrated photonic-electronic design method of claim 43 wherein:

the group IV semiconductor layer comprises silicon.

45. The integrated photonic-electronic design method of claim 43 wherein:

the group IV semiconductor layer comprises germanium.

46. The integrated photonic-electronic design method of claim 42 wherein:

the photonic interface comprises silicon.

47. The integrated photonic-electronic design method of claim 42 wherein:

the integrated photonic-electronic circuit is disposed on a silicon substrate, a silicon on quartz substrate, a silicon on sapphire substrate (SOS) or a silicon on insulator substrate (SOI).

48. The integrated photonic-electronic design method of claim 42 wherein:

the photonic interface comprises one or more receivers

for receiving optical signals from one or more of the optical fibers.

49. The integrated photonic-electronic design method of claim 48 wherein:

the receiver comprises one or more broad-band couplers.

50. The integrated photonic-electronic design method of claim 48 wherein:

the receiver comprises one or more detectors.

51. The integrated photonic-electronic design method of claim 48 wherein:

the receiver further comprises one or more optical filters.

52. The integrated photonic-electronic design method of claim 51 wherein:

the optical filter is an optical demultiplexer, a waveguide based filter, an Arrayed Waveguide (AWG) demultiplexer, a ring resonator demultiplexer or an add/drop filter.

53. The integrated photonic-electronic design method of claim 42 wherein:

the coupler comprises one or more transmitters for transmitting optical signals to one or more of the optical fibers.

54. The integrated photonic-electronic design method of claim 53 wherein:

the transmitter comprises one or more modulators.

55. The integrated photonic-electronic design method of claim 53 wherein:

the transmitter comprises one or more broad-band couplers.

56. The integrated photonic-electronic design method of claim 53 wherein:

the transmitter further comprises an optical filter.

57. The integrated photonic-electronic design method of claim 56 wherein:

the optical filter is an optical demultiplexer, a waveguide based filter, an Arrayed Waveguide (AWG) demultiplexer, a ring resonator demultiplexer, an optical multiplexer, an Arrayed Waveguide multiplexer, a ring resonator multiplexer or an add/drop filter.

58. The integrated photonic-electronic design method of claim 53 wherein:

the transmitter further comprises an optical power receiver for receiving optical power from an external optical power source.

59. The integrated photonic-electronic design method of claim 42 wherein:

light may be transmitted through the integrated photonic-electronic circuit through waveguides comprised of silicon.

60. The integrated photonic-electronic design method of claim 42 wherein:

the circuit portion comprises a processor.

61. The integrated photonic-electronic design method of claim 42 wherein:

the electronic circuit portion comprises a field programmable gate array (FPGA), a Programmable Logic Devices (PLD), or a Complex Programmable Logic Devices (CPLD).

62. The integrated photonic-electronic design method of claim 42 wherein: the electronic circuit portion comprises a memory module.

63. The integrated photonic-electronic design method of claim 42 wherein: the electronic circuit portion comprises analog circuits.

64. The integrated photonic-electronic design method of claim 42 wherein: the electronic circuit portion comprises radio frequency (RF) circuits.

65. The integrated photonic-electronic design method of claim 42 wherein: the electronic circuit portion comprises Complementary Metal Oxide Semiconductor (CMOS) circuits.

66. The integrated photonic-electronic design method of claim 42 wherein: the electronic circuit portion comprises Bipolar Complementary Metal Oxide Semiconductor (bi-CMOS) circuits.

67. The integrated photonic-electronic design method of claim 42 wherein: the electronic circuit portion comprises Hetero-Junction Biploar Transistor (HBT) circuits.

68. The integrated photonic-electronic design method of claim 42 wherein: the electronic circuit portion comprises a memory controller.

69. The integrated photonic-electronic design method of claim 42 wherein: the integrated photonic-electronic circuit is reconfigurable.

70. The integrated photonic-electronic design method of claim 42 wherein:

the photonic interface is reconfigurable.

71. The integrated photonic-electronic design method of claim 42 wherein:

the integrated photonic-electronic circuit is self-reconfiguring.

72. The integrated photonic-electronic design method of claim 42 wherein:

the integrated photonic-electronic circuit is introspective.

73 The integrated photonic-electronic design method of claim 42 wherein one or more of the optical fibers may be coupled to the top surface of the integrated photonic-electronic circuit surface.

74. The integrated photonic-electronic design method of claim 42 wherein one or more of the optical fibers may be coupled to the backside surface of the integrated photonic-electronic circuit surface.

75. The integrated photonic-electronic design method of claim 42 wherein one or more of the optical fibers may be coupled to the edge of the integrated photonic-electronic circuit surface.

76. The integrated photonic-electronic design method of claim 42 wherein the electronic portion may further comprise one or more electronic interfaces for electronically coupling to one or more electronic interconnects.

77. An integrated photonic-electronic circuit production process comprising the steps of:

providing a first circuit and a second circuit, each first and second circuit comprising:

an electronic circuit portion comprising at least one group IV semiconductor layer; and,

a photonic interface comprising silicon, the photonic interface integrated with the electronic circuit portion on a single chip, wherein the photonic interface comprises a coupler for coupling the circuit portion to one or more optical fiber, and wherein the photonic interface comprises at least one optical element for optical processing of light substantially in the plane of the single chip;

and

coupling the first circuit and the second circuit using one or more optical fibers.

78. The integrated photonic-electronic circuit production process of claim 77 wherein:

the first circuit comprises a processor, and the second circuit comprises a memory.

79. The integrated photonic-electronic circuit production process of claim 77 wherein:

at least one of the first and second circuits is reconfigurable.

80. The integrated photonic-electronic circuit production process of claim 77 wherein:

at least one of the first and second circuits is introspective.

81. The integrated photonic-electronic circuit production process of claim 77 wherein:

the group IV semiconductor layer comprises silicon.

82. The integrated photonic-electronic circuit production process of claim 77 wherein:

the group IV semiconductor layer comprises germanium.

83. The integrated photonic-electronic circuit production process of claim 77 wherein:

at least one coupler comprises one or more receivers

for receiving optical signals from one or more of the optical fibers.

84. The integrated photonic-electronic circuit production process of claim 83 wherein:

at least one receiver comprises one or more broad-band couplers.

85. The integrated photonic-electronic circuit production process of claim 83 wherein:

at least one receiver comprises one or more detectors.

86. The integrated photonic-electronic circuit production process of claim 83 wherein:

at least one receiver further comprises one or more optical filters.

87. The integrated photonic-electronic circuit production process of claim 86 wherein:

the optical filter is an optical demultiplexer, a waveguide based filter, an Arrayed WaveGuide (AWG) demultiplexer, ring resonator demultiplexer or an add/drop filter.

88. The integrated photonic-electronic circuit production process of claim 77 wherein:

at least one coupler comprises one or more transmitters for transmitting optical signals to one or more of the optical fibers.

89. The integrated photonic-electronic circuit production process of claim 88 wherein:

at least one transmitter comprises one or more modulators.

90. The integrated photonic-electronic circuit production process of claim 88 wherein:

at least one transmitter comprises one or more broad-band couplers.

91. The integrated photonic-electronic circuit production process of claim 88 wherein:

the transmitter comprises an optical filter.

92. The integrated photonic-electronic circuit production process of claim 91 wherein:

the optical filter is an optical demultiplexer, a waveguide based filter, an Arrayed WaveGuide (AWG) demultiplexer, ring resonator demultiplexer, an optical multiplexer, an Arrayed WaveGuide multiplexer, a ring resonator multiplexer or an add/drop filter.

93. The integrated photonic-electronic circuit production process of claim 88 wherein the transmitter comprises an optical power receiver for receiving optical power from an external optical power source.

94. The integrated photonic-electronic circuit production process of claim 93 wherein:

the external optical power source may comprise a substantially coherent light source.

95. The integrated photonic-electronic circuit production process of claim 93 wherein:

the external optical power source may comprise a partially incoherent light source.

96. The integrated photonic-electronic circuit production process of claim 93 wherein:

the external optical power source may comprise a single wavelength light source.

97. The integrated photonic-electronic circuit production process of claim 93 wherein:

the external optical power source may comprise a multiple wavelength light source.

98. The integrated photonic-electronic circuit production process of claim 93 wherein:

light may be transmitted through waveguides comprised of silicon in at least one of the first circuit or the second circuit.

99. The integrated photonic-electronic circuit production process of claim 77 wherein:

one or more of the optical fibers are coupled to the top surface of at least one of the first circuit or the second circuit.

100. The integrated photonic-electronic circuit production process of claim 77 wherein:

one or more of the optical fibers are coupled to the backside surface of at least one of the first circuit or the second circuit.

101. The integrated photonic-electronic circuit production process of claim 77 wherein:

one or more of the optical fibers are coupled to the edge of at least one of the first circuit or the second circuit.

102. The integrated photonic-electronic circuit production process of claim 77 wherein:

one or more of the optical fibers are coupled through a grating coupler to a surface of at least one of the first circuit or the second circuit.

103. The integrated photonic-electronic circuit production process of claim 77 wherein:

at least one circuit portion comprises one or more electronic interfaces for electronically coupling to one or more electronic interconnects.

104. An integrated photonic-electronic circuit comprising:

an electronic circuit portion comprising at least one group IV semiconductor layer; and

a photonic interface comprising silicon, wherein the photonic interface comprises a coupler for coupling the electronic circuit portion to one or more optical ports and wherein said coupler may process light substantially in the plane of the circuit;

wherein said integrated photonic-electronic circuit is integrated on a single chip.

105. The integrated photonic-electronic circuit of claim 104 wherein:

the group IV semiconductor layer comprises silicon.

106. The integrated photonic-electronic circuit of claim 104 wherein:

the group IV semiconductor layer comprises germanium.

107. The integrated photonic-electronic circuit of claim 104 wherein:

the single chip is a silicon substrate, silicon on quartz substrate, silicon on sapphire (SOS) substrate or silicon on insulator (SOI) substrate.

108. The integrated photonic-electronic circuit of claim 104 wherein:

the coupler comprises one or more receivers for receiving optical signals from one or more of the optical ports.

109. The integrated photonic-electronic circuit of claim 108 wherein:

the receiver comprises one or more broad-band couplers.

110. The integrated photonic-electronic circuit of claim 108 wherein:

the receiver comprises one or more detectors.

111. The integrated photonic-electronic circuit of claim 108 wherein:

the receiver further comprises one or more optical filters.

112. The integrated photonic-electronic circuit of claim 111 wherein:

the optical filter is an optical demultiplexer, a waveguide based filter, an Arrayed WaveGuide (AWG) demultiplexer, ring resonator demultiplexer or an add/drop filter.

113. The integrated photonic-electronic circuit of claim 104 wherein the coupler comprises one or more transmitters for transmitting optical signals to one or more of the optical ports.

114. The integrated photonic-electronic circuit of claim 113 wherein:

the transmitter comprises one or more modulators.

115. The integrated photonic-electronic circuit of claim 113 wherein:

the transmitter comprises one or more broad-band couplers.

116. The integrated photonic-electronic circuit of claim 113 wherein:

the transmitter further comprises one or more optical filters.

117. The integrated photonic-electronic circuit of claim 116 wherein:

the optical filter is an optical demultiplexer, a waveguide based filter, an Arrayed WaveGuide (AWG) demultiplexer, ring resonator demultiplexer, an add/drop filter, an optical multiplexer, an Arrayed WaveGuide multiplexer or an ring resonator multiplexer.

118. The integrated photonic-electronic circuit of claim 113 wherein:

the transmitter further comprises an optical power receiver for receiving optical power from an external optical power source.

119. The integrated photonic-electronic circuit of claim 118 wherein:

the external optical power source may comprise a substantially coherent light source.

120. The integrated photonic-electronic circuit of claim 118 wherein:

the external optical power source may comprise a partially incoherent light source.

121. The integrated photonic-electronic circuit of claim 118 wherein:

the external optical power source may comprise a single wavelength light source.

122. The integrated photonic-electronic circuit of claim 118 wherein:

the external optical power source may comprise a multiple wavelength light source.

123. The integrated photonic-electronic circuit of claim 104 wherein:

light may be transmitted through the integrated photonic-electronic circuit through waveguides comprised of silicon.

124. The integrated photonic-electronic circuit of claim 123 wherein:

the waveguides comprised of silicon are substantially in the plane of the chip.

125. The integrated photonic-electronic circuit of claim 104wherein:

the electronic circuit portion comprises a processor.

126. The integrated photonic-electronic circuit of claim 104 wherein:

the electronic circuit portion comprises a device selected from the group consisting of: a field programmable gate array (FPGA), a Programmable Logic Devices (PLD), or a Complex Programmable Logic Devices (CPLD).

127. The integrated photonic-electronic circuit of claim 104 wherein:

the electronic circuit portion comprises a memory module.

128. The integrated photonic-electronic circuit of claim 104 wherein:

the electronic circuit portion comprises analog circuits.

129. The integrated photonic-electronic circuit of claim 104 wherein:

the electronic circuit portion comprises radio frequency (RF) circuits.

130. The integrated photonic-electronic circuit of claim 104 wherein:

the electronic circuit portion comprises Complementary Metal Oxide Semiconductor (CMOS) circuits.

131. The integrated photonic-electronic circuit of claim 104 wherein:

the electronic circuit portion comprises Bipolar Complementary Metal Oxide Semiconductor (bi-CMOS) circuits.

132. The integrated photonic-electronic circuit of claim 104 wherein:

the electronic circuit portion comprises Hetero-Junction Biploar Transistor (HBT) circuits.

133. The integrated photonic-electronic circuit of claim 104 wherein:

the electronic circuit portion comprises a memory controller.

134. The integrated photonic-electronic circuit of claim 104 wherein:

the integrated photonic-electronic circuit is reconfigurable.

135. The integrated photonic-electronic circuit of claim 134 wherein:

the photonic interface is reconfigurable.

136. The integrated photonic-electronic circuit of claim 134 wherein:

the integrated photonic-electronic circuit is remotely reconfigurable.

137. The integrated photonic-electronic circuit of claim 134 wherein:

the integrated photonic-electronic circuit is self-reconfiguring.

138. The integrated photonic-electronic circuit of claim 104 wherein:

the integrated photonic-electronic circuit is introspective.

139. The integrated photonic-electronic circuit of claim 104 wherein:

one or more of the optical ports may be disposed on the top surface of the integrated photonic-electronic circuit.

140. The integrated photonic-electronic circuit of claim 104 wherein:

one or more of the optical ports may be coupled to one or more optical fibers.

141. The integrated photonic-electronic circuit of claim 104 wherein:

one or more of the optical ports may be disposed on the backside surface of the integrated photonic-electronic circuit.

142. The integrated photonic-electronic circuit of claim 104 wherein:

one or more of the optical ports may be disposed on an edge of the integrated photonic-electronic circuit.

143. The integrated photonic-electronic circuit of claim 104 wherein:

one or more of the optical ports may be coupled to optical fiber through a grating coupler disposed on a surface of the integrated photonic-electronic circuit.

144. The integrated photonic-electronic circuit of claim 104 further comprising:

one or more electronic interfaces for electronically coupling to one or more electronic interconnects.